VERTICAL DRAM PUNCHTHROUGH STOP SELF-ALIGNED TO STORAGE TRENCH

ABSTRACT OF THE DISCLOSURE

A semiconductor memory structure having a feature size of less than about 90 nm which exhibits little or no dynamic charge loss and little or no trap assisted junction leakage is provided. Specifically, the semiconductor structure includes at least one back-to-back pair of trench storage memory cells present in a Si-containing substrate. Each memory cell includes a vertical transistor overlaying a trench capacitor. Strap outdiffusions are present on each vertical sidewall of the trench storage memory cells so as to interconnect the vertical transistor and the trench capacitor of each memory cell to the Si-containing substrate. A punchthrough stop doping pocket is located between each back-to-back pair of trench storage memory cells and it is centered between the strap outdiffusions of adjacent storage trenches, and self-aligned to the adjacent storage trenches.